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FACSIMILE COVER SHEET

TO: EXAMINER PATEL (U.S. PATENT AND TRADEMARK OFFICE)

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FROM: MICHAEL W. TAYLOR, ESQ.

DATE: March 5, 2008

NUMBER OF PAGES (INCLUDING COVER SHEET): 35

COMMENTS/INSTRUCTIONS:

RE: U.S. PATENT APPLICATION SERIAL NO. 10/039,765

Attached is the following document:

1. Appellants' Appeal Brief

MAR 05 2008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: **ROCHE ET AL.**	
Serial No. **10/039,765**	Examiner: **N. PATEL**
Confirmation No. **9186**	Art Unit: **2111**
Filing Date: **November 7, 2001**	Attorney Docket No. **00RO30454288**
For: **SYNCHRONOUS DATA TRANSMISSION METHOD**	

APPELLANTS' APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellants' Appeal Brief together with the requisite $510.00 large entity fee for filing a brief. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. **01-0484**.

(1) Real Party in Interest

The real party in interest is STMicroelectronics S.A., assignee of the present application as recorded at reel 013215, frame 0699.

(2) Related Appeals and Interferences

At present there are no related appeals or interferences.

(3) Status of the Claims

Claims 20-46 and 48-52 are rejected in the application,

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all of which are being appealed herein.

(4) Status of the Amendments

All amendments have been entered and there are no further pending amendments. A copy of the claims involved in this appeal is attached hereto as Appendix A.

(5) Summary of the Claimed Subject Matter

The present invention, as recited in independent Claim 20, is directed to a method of transmitting data between two devices **D1**, **D2** via a clock line **CK** and at least one data line **DT**. See page 9, line 7 through page 10, line 31 and FIG. 1 of the present application (reproduced below).

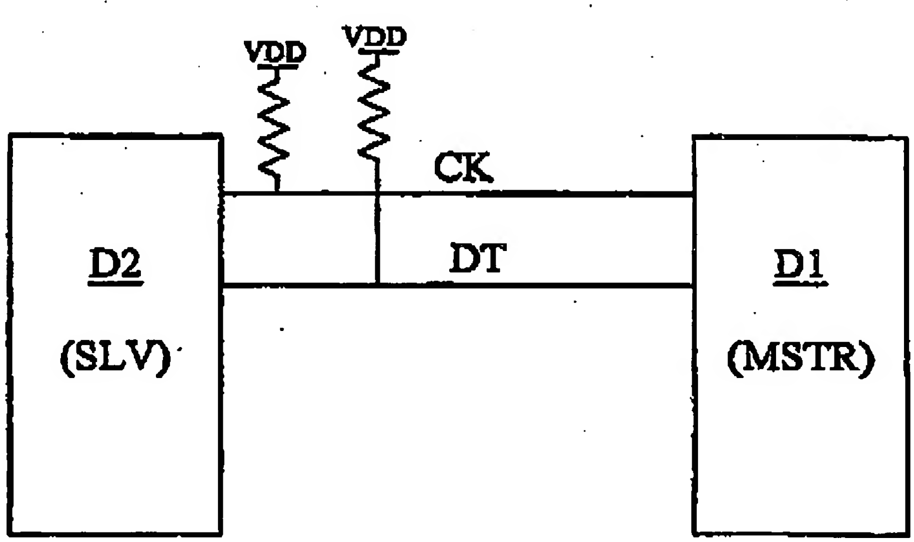

FIG. 1 of the Present Application

PAGE 4/35 * RCVD AT 3/5/2008 10:20:04 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-4/22 * DNIS:2738300 * CSID: * DURATION (mm-ss):08-32

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The clock line **CK** is maintained by default on a first logic value. The method comprises providing each device with the ability to tie the clock line **CK** to a potential representing a second logic value opposite the first logic value, and tying the clock line **CK** to the second logic value, via the two devices **D1** and **D2**, after data is applied to the data line **DT**. The tie to the clock line **CK** is maintained by the device **D1** or **D2** to which the data is sent while the device has not read the data. The data on the data line **DT** is maintained by the device **D2** or **D1** sending the data at least until an instant when the clock line **CK** is released by the device to which the data is sent.

The present invention may advantageously provide a double control of the line by which each device - a master **D1** or a slave **D2** - can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device **D1, D2** to impose its operating speed on the other, particularly in an event of disparity of clock frequencies or when one of the devices **D1** or **D2** operates in multitasking on applications that have priority over the data transmission itself.

Independent Claim 32 is directed to a method of transmitting data between two devices **D1, D2** connected via a clock line **CK** and at least one data line **DT**. See page 9, line 7 through page 10, line 31 and FIG. 1 of the present application (reproduced above). The method comprises maintaining the clock line **CK** on a first logic value as a default, and providing each device **D1, D2** with the ability to tie the clock line **CK** to a potential representing a second logic value. The clock line **CK** is tied to the second logic value, via the two devices **D1** and **D2**, after data is applied to the data line **DT**. The tie to the clock

line **CK** which the data is sent while the device **D1** or **D2** has not read the data is maintained. The data on the data line **DT** is maintained by the device **D2** or **D1** sending the data at least until the clock line **CK** is released by the device to which the data is sent.

Independent Claim 44 is directed to a data transmitting/receiving device **D1** or **D2**. See page 9, line 7 through page 10, line 31 and FIG. 1 of the present application (reproduced above). The data transmitting/receiving device **D1** or **D2** comprises a clock line connection terminal for connection to a clock line **CK**, and at least one data line connection terminal for connection to a data line **DT**. A circuit is for tying the clock line **CK** to a potential representing a second logic value that is the opposite of a first logic value. A data sending unit is for waiting for the clock line **CK** to have the first logic value, applying data to the data line **DT**, tying the clock line **CK** to the second logic value after the data is applied to the data line **DT**, and then releasing the clock line **CK**. The data on the data line **DT** is maintained by the data sending unit at least until the clock line **CK** has the first logic value, when the data is to be sent.

Independent Claim 46 is directed to a data transmitting/receiving device **D1** or **D2**. See page 9, line 7 through page 10, line 31 and FIG. 1 of the present application (reproduced above). The data transmitting/receiving device **D1** or **D2** comprises a clock line connection terminal for connection to a clock line **CK**, with the clock line being maintained by default on a first logic value. At least one data line connection terminal is for connection to a data line **DT**. A circuit is for tying the clock line **DT** to a potential representing a second logic value

that is the opposite of a first logic value. A detector is for detecting a change from the first logic value to the second logic value on the clock line **CK**, with the clock line being tied to the second logic value. The detector reads the data on the data line **DT**, and releases the clock line **CK** if data is to be received, or applies data to the data line **DT**, and releases the clock line **CK** if data is to be sent.

Independent Claim 48 is directed to a synchronous data transmission system. See page 9, line 7 through page 10, line 31 and FIG. 1 of the present application (reproduced above). The synchronous data transmission system comprises a clock line **CK**, a data line **DT**, and a master data transmitting/receiving device **D1**. The master data transmitting/receiving device **D1** comprises a clock line connection terminal connected to the clock line **CK**, at least one data line connection terminal connected to the data line **DT**, and a circuit for tying the clock line **CK** to a potential representing a second logic value that is the opposite of a first logic value. A data sending unit is for waiting for the clock line **CK** to have the first logic value, applying data to the data line **DT**, tying the clock line **CK** to the second logic value after the data is applied to the data line **DT**, then releasing the clock line **CK**. The data on the data line **DT** is to be maintained at least until the clock line **CK** has the first logic value, when the data is to be sent. The synchronous data transmission system further comprises a slave data transmitting/receiving device **D2** comprising a clock line connection terminal connected to the clock line **CK**, at least one data line connection terminal connected to the data line **DT**. A circuit is for tying the clock line **CK** to the potential representing the second logic value. A detector is for detecting a change from the first logic value to

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the second logic value on the clock line **CK**, tying the clock line **CK** to the second logic value, reading the data on the data line **DT**, and releasing the clock line **CK**, when the data is to be received.

Independent Claim 51 is directed to a communication interface circuit **HWC** for connection to a data transmitting/ receiving device **D1** or **D2** via a clock line **CK** and at least one data line **DT**. See page 18, line 16 through page 23, line 23 and FIG. 6 of the present application (reproduced below).

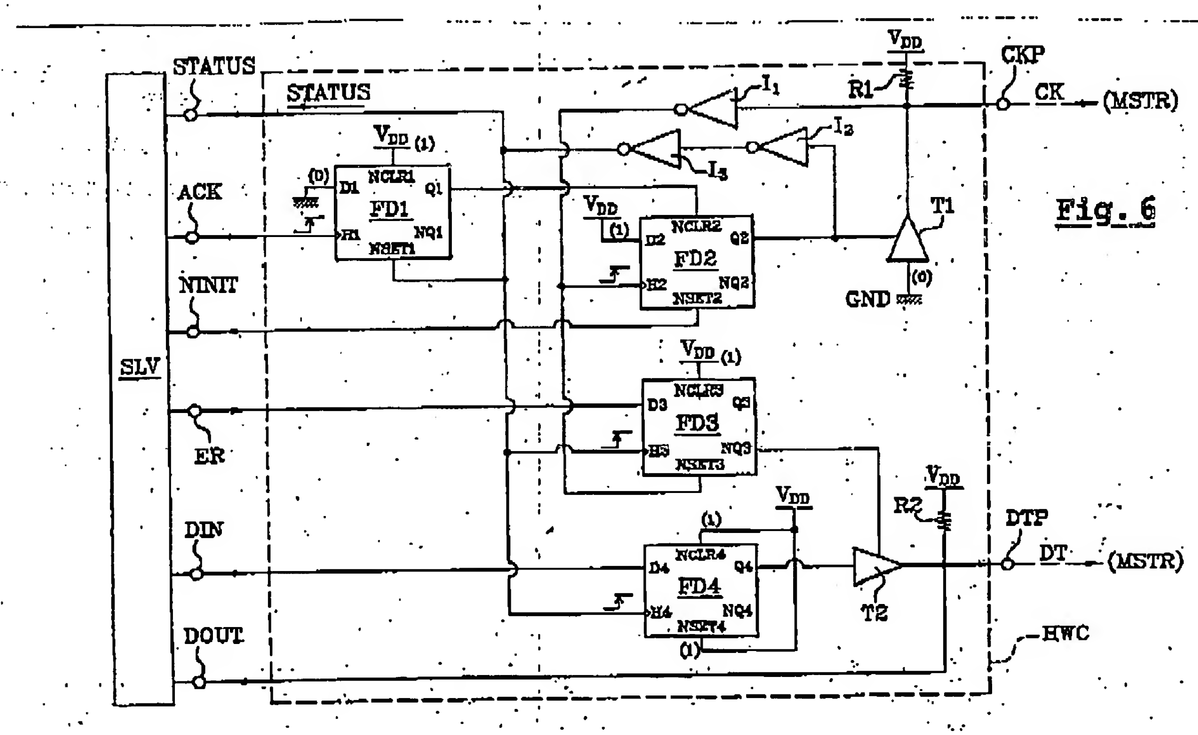

FIG. 6 of the Present Application

The communication interface circuit **HWC** comprises a circuit **FD1, FD2** for tying the clock line **CK** to a potential

representing a second logic value that is the opposite of a first logic value after data is applied to the at least one data line **DT**. A trigger (H input of **FD1** and **FD2**) is for automatically tying the clock line **CK** to the second logic value when the clock line is changing from the first logic value to the second logic value. An input **ACK** is to apply a clock line release signal to the trigger **FD1, FD2**. An output to deliver an information signal **STATUS** that has a first value when the clock line is tied to the second logic signal by the trigger and a second value when the clock line is released by the trigger.

(6) Grounds of Rejection to be Reviewed on Appeal

Claim 20-43 and 48-50 are rejected over the SPI Block Guide in view of the System Management Bus (SMBus) Specification.

Claims 44-46 are rejected over the SPI Block Guide.

Claims 51-52 are rejected over the SMBus Specification.

(7) Arguments

I. Independent Claims 20, 32 and 48 are Patentable over the SPI Block Guide in View of the SMBus Specification

The Examiner rejected independent Claims 20, 32 and 48 over the SPI Block Guide in view of the System Management Bus (SMBus) Specification. The Examiner has taken the position that FIG. 4-2 (reproduced below) on page 27 in the SPI Block Guide illustrates that the clock line is maintained by default on a first logic value (SCK=1), and that one of the devices has the ability to tie the clock line to a potential representing a second logic value opposite the first logic value (SCK=0 at SCK Edge No. 1).

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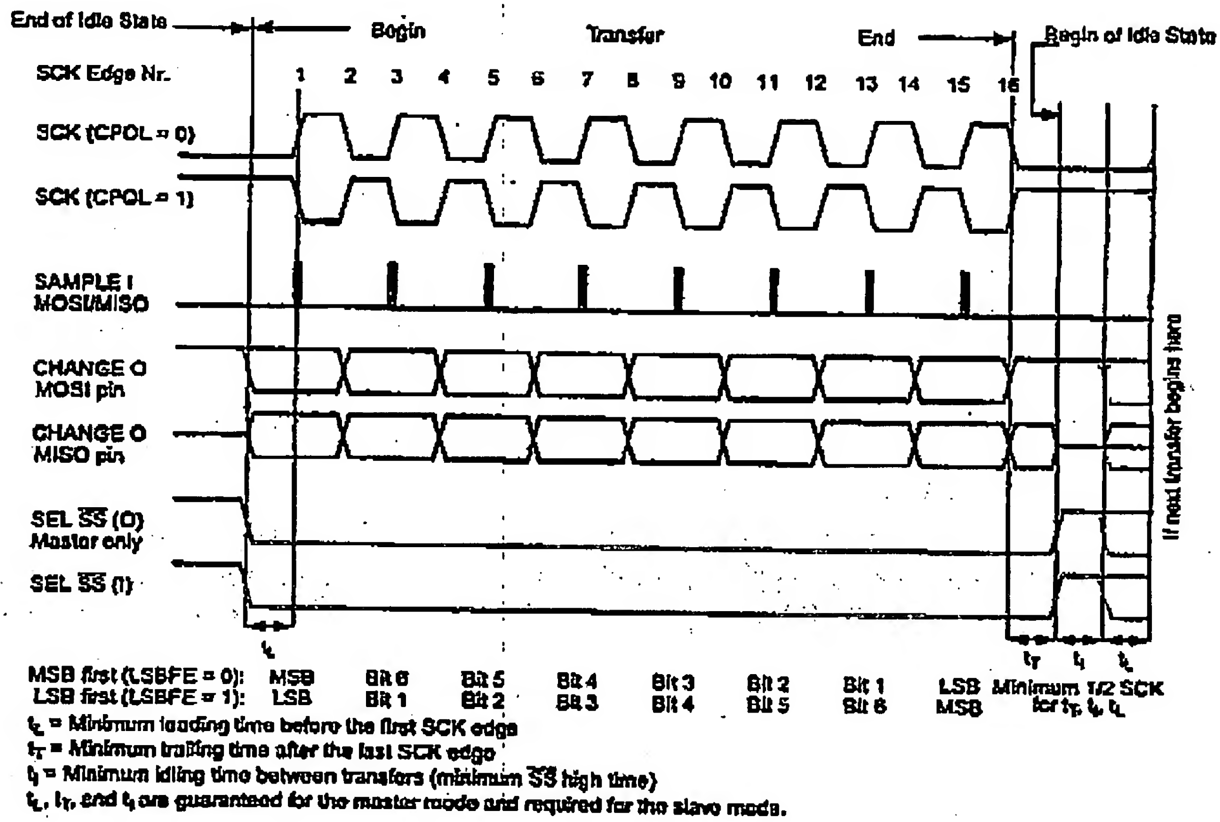

FIG. 4-2 of the SPI Block Guide

The Examiner also characterized the SPI Block Guide as disclosing that the clock line is tied to the second logic value, via the two devices, after data is applied to the data line (data is applied before SCK Edge No. 1), and data on the data line is maintained by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent (data is applied until rising edge of clock).

As correctly noted by the Examiner, the SPI Block Guide fails to disclose that the tie to the clock line is maintained by

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the device to which the data is sent while the device has not read the data. The Examiner cited the SMBus Specification as disclosing this feature. In particular, the Examiner referenced FIG. 4-7 (reproduced below) on page 22 in section 4.3.3. The Examiner has taken the position that it would have been obvious to have the device receiving data to hold the clock down, as disclosed by the SMBus Specification, in the method disclosed by the SPI Block Guide since this would allow clock synchronization so that slower slave devices could interface with faster masters.

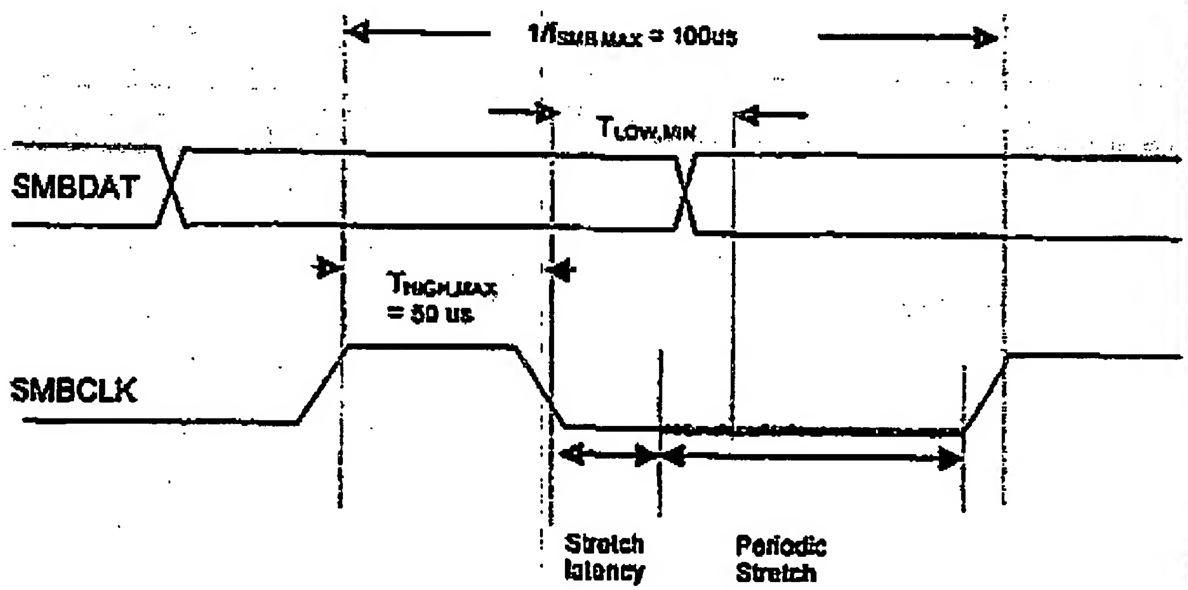

FIG. 4-7 of the SMBus Specification

The Applicants submit that even if the references were selectively combined as suggested by the Examiner, the claimed invention is still not provided. The clock line in the SPI Block

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Guide is under control of a master device. Reference is directed to FIG. 4-1 on page 26, for example, where there is no pull-up or pull-down of the clock SCK line. The clock is entirely under the control of the master device which uses a Baud Rate Generator to emit the clock signal. There is no tying of the clock signal from a default value to a second value. The slave, too, simply has a shift register to count the clock pulses, and thereby to synchronize itself to the clock signal.

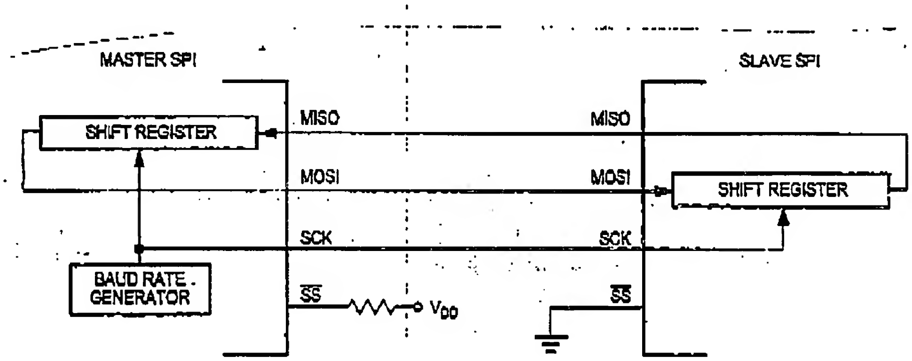

FIG. 4-1 of the SPI Block Guide

This is also confirmed on page 23, section 4.1, lines 11-12 in the SPI Block Guide, which provides: "When a data transfer operation is performed, this 16-bits register <u>is serially shifted eight positions by the S-clock from the master</u>, so data is exchanged between the master and the slave." (Emphasis added). Reference is also directed to page 24, section 4.3 titled "Slave Mode," lines 1-3, which provides: "The SPI operates in slave mode when the MSTR bit in SPI Control Regsiter1 is clear. - SCK Clock. In slave mode, <u>SCK is the SPI clock input from the master</u>." (Emphasis added).

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In other words, characterization of the SPI Block Guide by the Examiner is incorrect. The SPI Block Guide fails to teach or suggest the following that are in the claimed invention:

A) The clock line <u>is not</u> maintained by default on a first logic value;

B) Each device <u>is not provided</u> with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;

C) The two devices <u>do not tie</u> the clock line to the second logic value after data is applied to the data line;

D) The tying of the clock line <u>is not maintained</u> by the device to which the data is sent while the device has not read the data; and

E) The data on the data line <u>is not maintained</u> by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent.

In addition, the Examiner referenced FIG. 4-2 (reproduced above) on page 27 in the SPI Block Guide. The Applicants submit this figure is not relevant. In FIG. 4-2, the clock line SCK alternates between the high and the low state (when CPOL=1) but does not teach or suggest how the clock signal SCK is controlled by the devices exchanging data.

Referring now to the SMBus Specification, it appears that open drain lines are used with pull-up polarization (first logic value by default) and pull-down control for sending data having the "second logic value opposite the first logic value". As to the open drain line configuration of the SMBDAT line (data line) and SMBCLK line (clock line), see for example page 9, FIG. 2-1 (reproduced below), and page 10, FIGS. 2-2, 2-3 (reproduced below) plus the corresponding descriptions associated with these figures.

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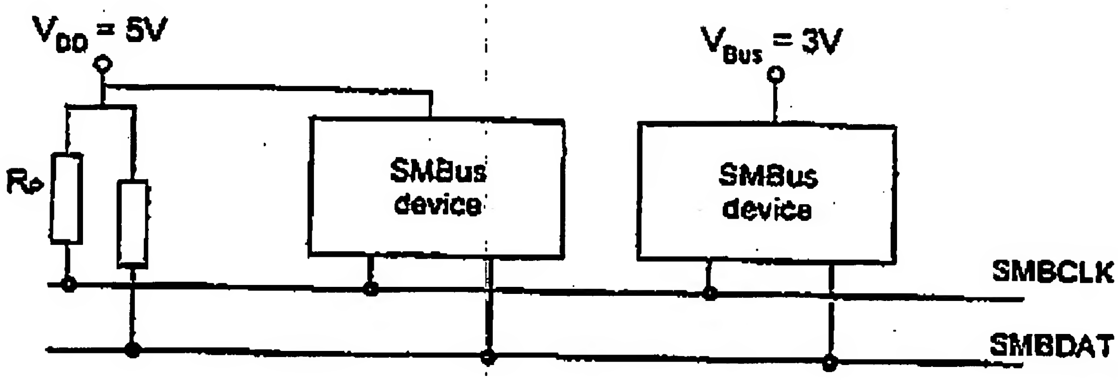

FIG. 2-1 of the SMBus Specification

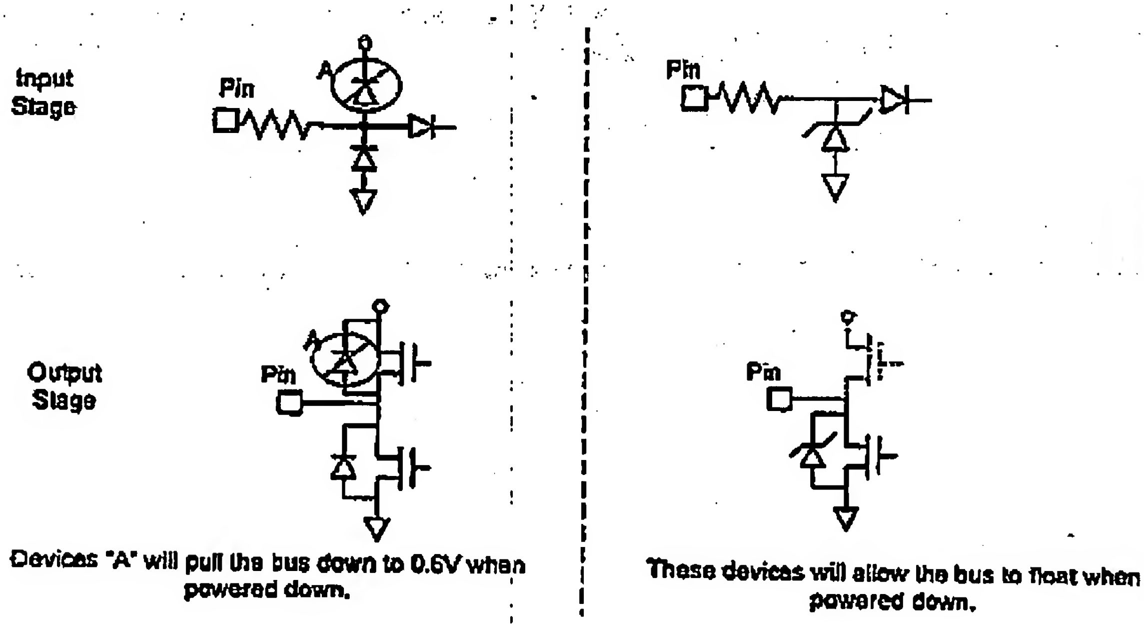

FIG. 2-2 of the SMBus Specification

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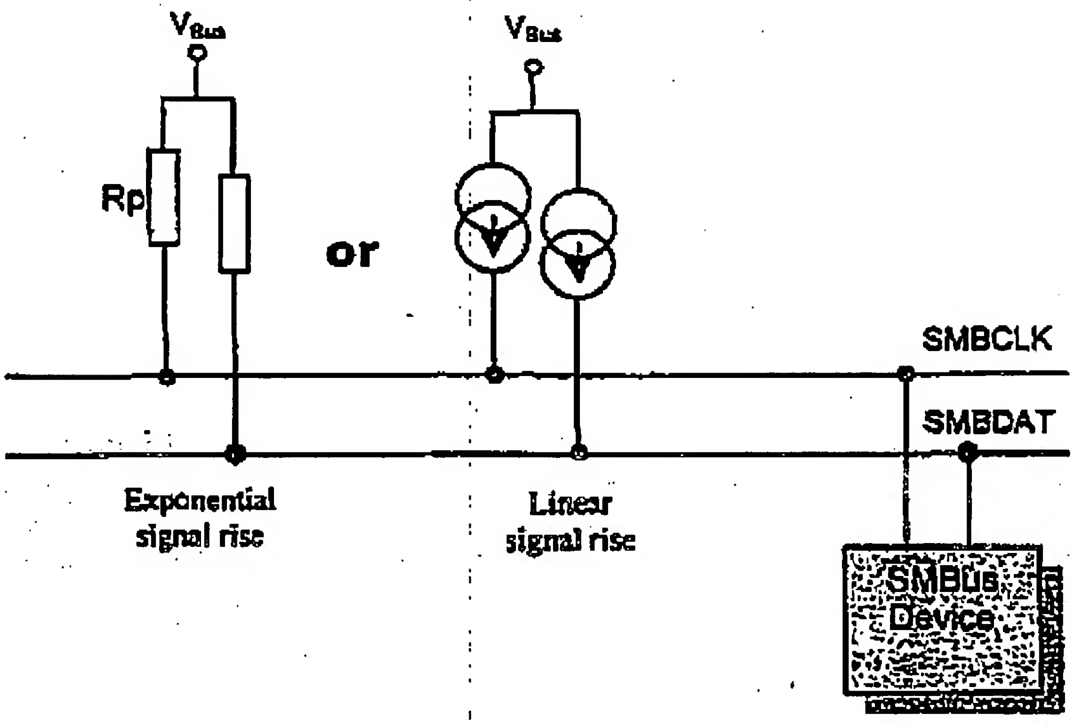

FIG. 2-3 of the SMBus Specification

In other words, the SMBus Specification fails to teach or suggest tying the clock line to the second logic value, via the two devices, after data is applied to the data line. Referring to page 9, lines 2-3, which provides "Generally, a bus master device initiates a bus transfer between it and a single bus slave and <u>provides the clock signals</u>." (Emphasis added). Reference is also directed to page 20, section 4.3.1 titled Synchronization, lines 5-6, which provides: "A high-to-low transition on the SMBCLK line will cause all devices involved to

start counting off their LOW period and start driving SMBCLK low if the device is a master".

The SMBus Specification fails to teach or suggest that both the master and the slave device can tie the clock line to a second logic value opposite the first logic value. Instead, only the master device can tie the clock line to a different potential.

Moreover, the SMBus Specification fails to teach or suggest that the tie to the clock line by the device to which the data is sent is maintained while the device has not read the data. Even though the SMBus Specification discloses that a slave device may stretch the clock period, the slave must comply with a certain timeout.

Referring to page 12, note 5, which provides: "It is possible that a slave device or another master will also extend the clock causing the combined clock low time to be greater than TLOW-MEXT" (i.e., Cumulative Clock Low Extended Time allowed to the Master device, see TABLE on page 12). Reference is also directed to page 13 section 3.1.1.3 titled "Slave device timeout definition and conditions," which provides: "It is highly recommended that a slave device release the bus when it detects a single clock held low longer than Ttimeout, min".

Reference is also directed to page 22, section 4.3.3 (which the Examiner also references), lines 2-3, which provides: "In addition to the bus arbitration procedure the clock synchronization mechanism can be used during a bit or a byte transfer in order to allow a slower slave device to cope with faster masters". As illustrated in FIG. 4-7 on page 22, Clock LOW extension, or stretching, if necessary, must start after the SMBCLK high-to-low transition. A slave device may opt to stretch the clock line during a specific bit transfer in order to process

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a real time task or check the validity of a byte. In this case the slave must adhere to the timeout specifications. A slave device may select to stretch the clock LOW period between byte transfers on the bus in order to process received data or prepare data for transmission.

The SMBus Specification provides a data transfer method on open drain lines which is very different from the claimed invention. In the SMBus Specification, data is stable and is read when the clock signal has a default value (e.g., HIGH since the SMBus Specification provides only a pull-up polarization of the lines), and data is changed when the clock signal is tied to an opposite value (e.g., LOW).

In sharp contrast, the present invention provides a double control of the line by which each device - a master or a slave - can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly in the event of disparity of clock frequencies or when one of the devices operates in multitasking on applications that have priority over the data transmission itself.

Accordingly, it is submitted that independent Claim 20 is patentable over the SPI Block Guide in view of the SMBus Specification. Independent Claims 32 and 48 are similar to independent Claim 20. It is submitted that independent Claims 32 and 48 are also patentable over the SPI Block Guide in view of the SMBus Specification.

II. Independent Claims 44 and 46 are Patentable over the SPI Block Guide

The Examiner rejected independent Claims 44 and 46 over the SPI Block Guide. As noted above, the Examiner has taken the

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position that FIG. 4-2 in the SPI Block Guide discloses a data transmitting/receiving device comprising a clock line connection terminal for connection to a clock line, and at least one data line connection terminal for connection to a data line. The Examiner has also taken the position that the SPI Block Guide discloses a circuit for tying the clock line to a potential representing a second logic value (low) that is opposite of a first logic value(high) (SCK changes from 1 to 0 at SCK Edge Nr. 1), and a data sending unit as also in the claimed invention.

The clock line in the SPI Block Guide is under control of a master device. Reference is directed to FIG. 4-1 on page 26, for example, where there is no pull-up or pull-down of the clock SCK line. The clock is entirely under the control of the master device which uses a Baud Rate Generator to emit the clock signal. There is no tying of the clock signal from a default value to a second value. The slave, too, simply has a shift register to count the clock pulses, and thereby to synchronize itself to the clock signal.

This is also confirmed on page 23, section 4.1, lines 11-12 in the SPI Block Guide, which provides: "When a data transfer operation is performed, this 16-bits register <u>is serially shifted eight positions by the S-clock from the master</u>, so data is exchanged between the master and the slave." (Emphasis added). Reference is also directed to page 24, section 4.3 titled "Slave Mode," lines 1-3, which provides: "The SPI operates in slave mode when the MSTR bit in SPI Control Regsiter1 is clear. - SCK Clock. In slave mode, <u>SCK is the SPI clock input from the master</u>." (Emphasis added).

In other words, characterization of the SPI Block Guide by the Examiner is incorrect. The SPI Block Guide fails to teach or suggest the following with respect to the data sending unit:

1) waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value after the data is applied to the data line, then releasing the clock line, and 2) maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent.

In addition, the Examiner referenced FIG. 4-2 on page 27 in the SPI Block Guide. The Applicants submit this figure is not relevant. In FIG. 4-2, the clock line SCK alternates between the high and the low state (when CPOL=1) but does not teach or suggest how the clock signal SCK is controlled by the devices exchanging data.

In sharp contrast, the present invention provides a double control of the line by which each device - a master or a slave - can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly in the event of disparity of clock frequencies or when one of the devices operates in multitasking on applications that have priority over the data transmission itself.

Accordingly, it is submitted that independent Claim 44 is patentable over the SPI Block Guide. Independent Claim 46 is similar to independent Claim 44. It is submitted that independent Claim 46 is also patentable over the SPI Block Guide.

III. Independent Claim 51 is Patentable over the SMBus Specification

The Examiner rejected independent Claim 51 over the SMBus Specification. The Examiner has taken the position that FIG. 4-8 (reproduced below) on page 22 in the SMBus Specification illustrates the claimed invention.

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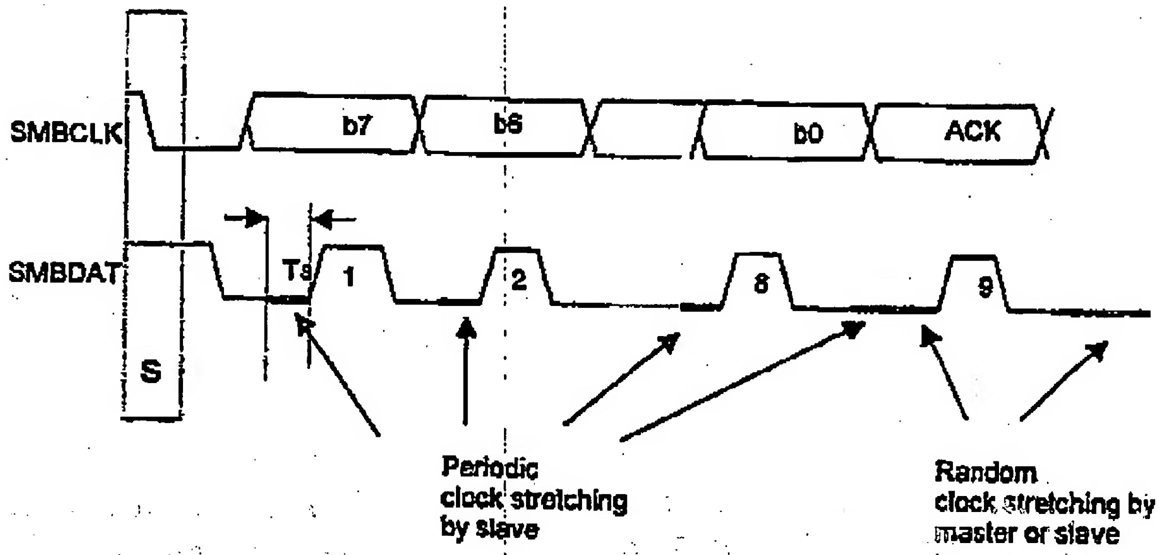

FIG. 4-8 of the SMBus Specification

As discussed above, in the SMBus Specification, it appears that open drain lines are used with pull-up polarization (first logic value by default) and pull-down control for sending data having the "second logic value opposite the first logic value". As to the open drain line configuration of the SMBDAT line (data line) and SMBCLK line (clock line), see for example page 9, FIG. 2-1, and page 10, FIGS. 2-2, 2-3 plus the corresponding descriptions associated with these figures.

The SMBus Specification fails to teach or suggest a trigger for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value, an input to apply a clock line release signal to the trigger, and an output to deliver an

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information signal that has a first value when the clock line is tied to the second logic signal by the trigger and a second value when the clock line is released by the trigger as in the claimed invention.

More particularly, such a trigger is not disclosed because the SMBus Specification fails to teach or suggest tying the clock line to the second logic value, via two devices, after data is applied to the data line. Referring to page 9, lines 2-3, which provides "Generally, a bus master device initiates a bus transfer between it and a single bus slave and <u>provides the clock signals</u>." (Emphasis added). Reference is also directed to page 20, section 4.3.1 titled Synchronization, lines 5-6, which provides: "A high-to-low transition on the SMBCLK line will cause all devices involved to start counting off their LOW period and start driving SMBCLK low <u>if</u> the device is a master".

The SMBus Specification fails to teach or suggest that <u>both</u> the master and the slave device can tie the clock line to a second logic value opposite the first logic value. Instead, only the master device can tie the clock line to a different potential. Moreover, the SMBus Specification fails to teach or suggest that the tie to the clock line by the device to which the data is sent is maintained while the device has not read the data. Even though the SMBus Specification discloses that a slave device may stretch the clock period, the slave must comply with a certain timeout.

Referring to page 12, note 5, which provides: "It is possible that a slave device or another master will also extend the clock causing the combined clock low time to be greater than TLOW-MEXT" (i.e., Cumulative Clock Low Extended Time allowed to the Master device, see TABLE on page 12). Reference is also directed to page 13 section 3.1.1.3 titled "Slave device timeout

definition and conditions," which provides: "It is highly recommended that a slave device release the bus when it detects a single clock held low longer than Ttimeout, min".

Reference is also directed to page 22, section 4.3.3 (which the Examiner also references), lines 2-3, which provides: "In addition to the bus arbitration procedure the clock synchronization mechanism <u>can be used</u> during a bit or a byte transfer <u>in order to allow a slower slave device to cope with faster masters</u>". As illustrated in FIG. 4-7 on page 22, Clock LOW extension, or stretching, <u>if necessary</u>, must start after the SMBCLK high-to-low transition. A slave device <u>may opt to stretch the clock</u> line during a specific bit transfer <u>in order to process a real time task or check the validity of a byte</u>. <u>In this case the slave must adhere to the timeout specifications</u>. A slave device may select to stretch the clock LOW period <u>between byte transfers</u> on the bus in order to process received data or prepare data for transmission.

The SMBus Specification provides a data transfer method on open drain lines which is very different from the claimed invention. In the SMBus Specification, data is stable and is read when the clock signal has a default value (e.g., HIGH since the SMBus Specification provides only a pull-up polarization of the lines), and data is changed when the clock signal is tied to an opposite value (e.g., LOW).

In sharp contrast, the present invention provides a trigger as part of a communication interface circuit for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value, an input to apply a clock line release signal to the trigger, and an output to deliver an information signal that has a first value when the clock line is tied to the second

logic signal by the trigger and a second value when the clock line is released by the trigger. This allows for a double control of the line by which each device - a master or a slave - can be considered as a master as far as the duration of the clock period is concerned. This advantageously allows each device to impose its operating speed on the other, particularly in the event of disparity of clock frequencies or when one of the devices operates in multitasking on applications that have priority over the data transmission itself.

Accordingly, it is submitted that independent Claim 51 is patentable over the SMBus Specification.

IV. Conclusions

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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Filing Date: **November 7, 2001**

Attorney for Appellant

CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 5th day of March, 2008.

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APPENDIX A - CLAIMS ON APPEAL FOR U.S. PATENT APPLICATION SERIAL NO. 10/039,765

20. A method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value, the method comprising:

providing each device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;

tying the clock line to the second logic value, via the two devices, after data is applied to the data line;

maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data; and

maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent.

21. A method according to Claim 20, wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted.

22. A method according to Claim 21, wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device.

23. A method according to Claim 22, wherein the slave

device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device.

24. A method according to Claim 23, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line.

25. A method according to Claim 21, wherein the master device ties the clock line to the second logic value when the master receives data from the slave device.

26. A method according to Claim 25, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device.

27. A method according to Claim 26, wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line.

28. A method according to Claim 21, wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value

is independent of any action by the slave device.

29. A method according to Claim 21, further comprising providing the slave device with a communication interface circuit including:

a trigger for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value;

an input for applying a clock line release signal to the trigger; and

an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger and a second value when the clock line is released by the trigger.

30. A method according to Claim 29, wherein the communication interface circuit further comprises:

storage for storing at least one data; and

an applicator for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value.

31. A method according to Claim 20, wherein the first logic value is 1 and the second logic value is 0.

32. A method of transmitting data between two devices connected via a clock line and at least one data line, the method comprising:

maintaining the clock line on a first logic value as a default;

providing each device with the ability to tie the clock

line to a potential representing a second logic value;

tying the clock line to the second logic value, via the two devices, after data is applied to the data line;

maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data; and

maintaining the data on the data line by the device sending the data at least until the clock line is released by the device to which the data is sent.

33. A method according to Claim 32, wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted.

34. A method according to Claim 33, wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device.

35. A method according to Claim 34, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device.

36. A method according to Claim 35, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the

slave device has not released the clock line.

37. A method according to Claim 33, wherein the master device ties the clock line to the second logic value when the master receives data from the slave device.

38. A method according to Claim 37, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device.

39. A method according to Claim 38, wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line.

40. A method according to Claim 33, wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device.

41. A method according to Claim 33, further comprising providing the slave device with a communication interface circuit including:

a trigger circuit for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value;

an input for applying a clock line release signal to

the trigger circuit; and

an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger circuit and a second value when the clock line is released by the trigger circuit.

42. A method according to Claim 41, wherein the communication interface circuit further comprises:

a buffer for storing at least one data; and

a circuit for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value.

43. A method according to Claim 32, wherein the first logic value is 1 and the second logic value is 0.

44. A data transmitting/receiving device comprising:

a clock line connection terminal for connection to a clock line;

at least one data line connection terminal for connection to a data line;

a circuit for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value; and

a data sending unit for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value after the data is applied to the data line, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent.

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45. A device according to Claim 44, further comprising a data receiving unit for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading data on the data line, then releasing the clock line, when the data is to be received.

46. A data transmitting/receiving device comprising:

a clock line connection terminal for connection to a clock line, the clock line being maintained by default on first logic value;

at least one data line connection terminal for connection to a data line;

a circuit for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value; and

a detector for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, and

reading the data on the data line, and releasing the clock line if data is to be received, or

applying data to the data line, and releasing the clock line if data is to be sent.

Claim 47 (Cancelled).

48. A synchronous data transmission system comprising:
a clock line;
a data line;
a master data transmitting/receiving device comprising

a clock line connection terminal connected to the clock line,

at least one data line connection terminal connected to the data line,

a circuit for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value, and

a data sending unit for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value after the data is applied to the data line, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent; and

a slave data transmitting/receiving device comprising

a clock line connection terminal connected to the clock line;

at least one data line connection terminal connected to the data line;

a circuit for tying the clock line to the potential representing the second logic value; and

a detector for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, reading the data on the data line, and releasing the clock line, when the data is to be received.

49. A system according to Claim 48, wherein the master device further comprises a data receiving unit for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading the data on the data line, then releasing the clock line, when the data is to be received by the master device.

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50. A system according to Claim 48, wherein the slave device further comprises a detector for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line the second logic value, applying the data to the data line, and releasing the clock line, when the data is to be sent from the slave device.

51. A communication interface circuit for connection to a data transmitting/receiving device via a clock line and at least one data line, the circuit comprising:

a circuit for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value after data is applied to the at least one data line;

a trigger for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value;

an input to apply a clock line release signal to the trigger; and

an output to deliver an information signal that has a first value when the clock line is tied to the second logic signal by the trigger and a second value when the clock line is released by the trigger.

52. A communication interface circuit according to Claim 51 further comprising:

storage for storing data; and

an applicator for automatically applying the data to the data line when the clock line changes from the first logic value to the second logic value.

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APPENDIX B – EVIDENCE APPENDIX
PURSUANT TO 37 C.F.R. § 41.37(c)(1)(ix)

None.

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APPENDIX C - RELATED PROCEEDINGS APPENDIX PURSUANT TO 37 C.F.R. § 41.37(c)(1)(x)

None.